PATENT
ATTORNEY DOCKET NO.: 46969-5313

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Hideki KOBAYASHI	)	Confirmation No.: 6306
	)	
Application No.: 10/701,080	)	Group Art Unit: 2627
	)	
Filed: November 5, 2003	)	Examiner: Gautam Patel
	)	
For: INFORMATION RECORDING/REPRODUCING APPARATUS AND INFORMATION REPRODUCING METHOD (As Amended)	)	

USPTO Customer Service Window, **Mail Stop AF**
Randolph Building
401 Dulany Street
Alexandria, Virginia 22314

REQUEST FOR PRE-APPEAL BRIEF CONFERENCE

Dear Sir:

Applicants respectfully request a pre-appeal brief conference for the reasons set forth below.

Applicants respectfully submit that clear errors exist in the Examiner's final rejection of claims 1, 4, 7, 8 and 11 under 35 U.S.C. § 102(b) based on U.S. Patent No. 6,172,952 to Inokuchi et al. Specifically, Applicants respectfully submit that Inokuchi does not teach or suggest any feature relating to the claimed operations that are performed when "the corrected address data is determined as a correct address" as recited in independent claims 1, 7 and 8 of the present application.

Applicants note that independent claims 1 and 7 recite an address judging section for determining whether or not the corrected address data is a correct address and, when the

corrected address data is determined as a correct address, "the synchronization process is put into stand-by for execution until the corrected address data is determined as an incorrect address." Similar limitations are recited in independent claim 8.

Applicants submit, however, that in Inokuchi, abnormality detection is performed based on the phase relationship between the synchronization clock generated by the PLL circuit and the signal generated from the wobble signal. Therefore, in Inokuchi, the synchronization clock signal and the signal generation from the wobble signal must always be monitored in order to detect an abnormality. In contrast, in the claimed embodiments of the present invention, the synchronization of the reproduced signal is not monitored when the address is determined to be correct (the synchronization process is put in stand-by).

Applicants further note that the Examiner states in the Office Action that PLL circuits are well known in the art. However, Applicants submit that the claimed embodiments of the present invention are not particular to a PLL circuit.

Also, Applicants note that in Inokuchi, the synchronization operation is held when the optical head is moving across the tracks of the optical disc. Column 16, lines 29-49 of Inokuchi describe timings in which the charge pump 18 holds the synchronization operation. Applicants submit that these timings are completely different from the period in which the synchronization operation is placed in a stand-by state in the claimed embodiments of the present invention (when the address is determined to be correct).

Hence, Applicants submit that for at least these reasons, Inokuchi fails to anticipate the embodiments of the present invention even as recited in independent claims 1, 7 and 8.

For all the reasons given above and previously, Applicants respectfully request that this rejection be withdrawn and the application be allowed.

Respectfully submitted,
DRINKER BIDDLE & REATH LLP

Dated: January 17, 2008

By: _____
Joseph J. Buczynski
Reg. No. 35,084

Customer No. 055694
DRINKER BIDDLE & REATH LLP
1500 K Street, N.W., Suite 1100
Washington, DC 20005-1209
Tel.: (202) 230-5114
Fax: (202) 842-8465

DC01/ 535890.1